DETAILED ACTION

This Examiner's Amendment & Examiner's Reasons for Allowance action is in response to the filing of 04/15/2009.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Andre M. Szuwalski (35,701) on 10/15/2009.

The application has been amended as follows:

Claim 1. (Currently Amended) An electronic component, comprising:

an integrated circuit embodied on a single monolithic substrate and incorporating:

a tuning circuit of the direct sampling type including mixed analog and digital circuitry configured to receive RF satellite digital television signals composed of several channels at a circuit input for direct sampling at RF and digital transposition to output several downconverted signals each associated with a different selected channel; and

several channel decoding digital circuits connected at the outputs of the tuning circuit and each including digital circuitry to deliver respectively and simultaneously several streams of data packets corresponding to the different selected channels;

wherein the analog circuitry of the tuning circuit is fabricated in a first portion of that single monolithic substrate and digital circuitry of the tuning circuit and the several channel decoding circuits are fabricated in a second portion of that single monolithic substrate; and

a semiconducting barrier formed in the single monolithic substrate between the first portion and the second portion to insulate the analog circuitry in the first portion from noise on a supply voltage for the digital circuitry in the second portion;

wherein the channels extend over a predetermined frequency span and the RF signals convey digital information coded by digital modulation, and

wherein each channel decoding digital circuit comprises:

a low pass digital decimator filter followed by an additional digital filter for eliminating information of adjacent channels, the additional digital filter having a cutoff frequency of the order of the frequency half-width of a channel; and

a digital error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel being processed by the channel decoding module.

Claim 2. (Previously Presented) The component according to Claim 1, wherein the channels extend over a predetermined frequency span and the RF signals convey digital information coded by digital modulation, and

wherein the tuning circuit comprises:

an analog stage receiving the RF signals;

a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the frequency span of the sampled RF signal; and

several digital devices for transposing frequencies that are connected to the output of the analog conversion stage, each digital device configured to separately deliver a sampled digital signal centered at the zero frequency and corresponding to the selected channel.

Claim 3. (Canceled).

Claim 4. (Currently Amended) An electronic ~~The~~ component ~~according to Claim 1~~, comprising:

an integrated circuit embodied on a single monolithic substrate and incorporating:

a tuning circuit of the direct sampling type including mixed analog and digital circuitry configured to receive RF satellite digital television signals composed of several channels at a circuit input for direct sampling at RF and digital transposition to output several downconverted signals each associated with a different selected channel; and

several channel decoding digital circuits connected at the outputs of the tuning circuit and each including digital circuitry to deliver respectively and simultaneously several streams of data packets corresponding to the different selected channels;

wherein the analog circuitry of the tuning circuit is fabricated in a first portion of that single monolithic substrate and digital circuitry of the tuning circuit and the several channel decoding circuits are fabricated in a second portion of that single monolithic substrate; and

a semiconducting barrier formed in the single monolithic substrate between the first portion and the second portion to insulate the analog circuitry in the first portion from noise on a supply voltage for the digital circuitry in the second portion;

wherein the channels extend over a predetermined frequency span and the RF signals convey digital information coded by digital modulation, and

wherein the tuning circuit comprises:

an analog stage receiving the RF signals;

a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the frequency span of the sampled RF signals; and

several digital devices for transposing frequencies that are connected to the output of the analog conversion stage, each digital device configured to separately deliver a sampled digital signal centered at the zero frequency and corresponding to the selected channel; and

wherein each channel decoding digital circuit comprises:

a low pass digital decimator filter followed by an additional digital filter for eliminating information of adjacent channels, the additional digital filter having a cutoff frequency of the order of the frequency half-width of a channel; and

a digital error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel associated with the sampled digital signal processed by this channel decoding circuit.

Claim 5. (Original) The component according to Claim 4, wherein the resolution of the analog/digital conversion stage is greater than or equal to 6 bits.

Claim 6. (Currently Amended) ~~An electronic~~ The component according to Claim 4, ~~comprising: an integrated circuit embodied on a single monolithic substrate and incorporating: a tuning circuit of the direct sampling type including mixed analog and digital circuitry configured to receive RF satellite digital television signals composed of several channels at a circuit input for direct sampling at RF and digital transposition to output several downconverted signals each associated with a different selected channel; and several channel decoding digital circuits connected at the outputs of the tuning circuit and each including digital circuitry to deliver respectively and simultaneously several streams of data packets corresponding to the different selected channels; wherein each channel decoding digital circuit comprises a digital decimator filter followed by an additional digital filter for eliminating information of adjacent channels; wherein the tuning circuit and the several channel decoding circuits are fabricated on that single monolithic substrate; and~~ wherein the decimator filter is a low-pass filter whose cutoff frequency is of the order of twice the frequency half-width of a channel, and wherein the cutoff frequency of the additional digital filter is of the order of the frequency half-width of a channel.

Claim 7. (Currently Amended) ~~An electronic~~ The component according to Claim 1, further comprising: ~~an integrated circuit embodied on a single monolithic substrate and incorporating: a tuning circuit of the direct sampling type including mixed analog and digital circuitry configured to receive RF satellite digital television signals composed of several channels at a circuit input for direct sampling at RF and digital transposition to output several downconverted signals each associated with a different selected channel; and several channel decoding digital circuits connected at the outputs of the tuning circuit and each including digital~~

~~circuitry to deliver respectively and simultaneously several streams of data packets corresponding to the different selected channels;~~

a grounding metal plate glued to a rear face of the single monolithic substrate by a conducting glue to provide a high frequency current spike absorbing capacitor having a first plate formed of the substrate and a second plate formed of the metal plate with an oxide dielectric there between ~~; and wherein the tuning circuit and the several channel decoding circuits are fabricated on that single monolithic substrate~~.

Claim 8. (Previously Presented) The component according to Claim 1, wherein the substrate has a first type of conductivity and the digital circuitry of the tuning circuit and several channel decoding digital circuits are disposed in the second portion of the substrate that is insulated from the first portion of the substrate for the analog circuitry by the semiconducting barrier having a second type of conductivity different from the first type of conductivity, and wherein the semiconducting barrier is biased by a bias voltage different from the supply voltage for the digital circuitry.

Claim 9. (Original) The component of Claim 1, wherein the electronic component comprises a satellite digital television signal receiver.

Claim 10. (Previously Presented) An integrated circuit, comprising:

a single monolithic substrate in which the following circuit components are provided:

an input receiving an RF analog signal including a plurality of channels;

an analog-to-digital converter to sample and convert the RF analog signal to a digital signal;

a first digital tuner that downconverts the digital signal to a first downconverted digital signal, wherein information of a selected first channel in the downconverted digital signal is centered at zero frequency;

a first channel decoding digital circuit connected to the first digital tuner that digitally decodes the first downconverted digital signal to output a stream of data packets for the selected first channel;

a second digital tuner that downconverts the digital signal to a second downconverted digital signal, wherein information of a selected second channel in the downconverted digital signal is centered at zero frequency; and

a second channel decoding digital circuit connected to the second digital tuner that digitally decodes the second downconverted digital signal to output a stream of data packets for the selected second channel;

a grounding metal plate glued to a rear face of the single monolithic substrate by a conducting glue to provide a high frequency current spike absorbing capacitor having a first plate formed of the substrate and a second plate formed of the metal plate with an oxide dielectric there between;

wherein circuitry of the converter, tuners and channel decoding digital circuits are fabricated on that single monolithic substrate.

Claim 11. (Previously Presented) The circuit of claim 10 wherein the first and second digital tuners perform frequency transposition and channel selection in a digital domain.

Claim 12. (Previously Presented) The circuit of claim 10 wherein the analog-to-digital converter oversamples the received RF analog signal.

Claim 13. (Previously Presented) The circuit of claim 10 wherein the RF analog signal conveys information for the plurality of channels by digital modulation.

Claim 14. (Previously Presented) The circuit of claim 10 wherein the channels of the RF analog signal extend over a frequency span and wherein the analog-to-digital converter oversamples the received RF analog signal at a sampling frequency at least twice the frequency span.

Claim 15. (Previously Presented) The circuit of claim 14 wherein the RF analog signal comprises a satellite digital television analog signal.

Claim 16. (Previously Presented) The circuit of claim 10 wherein each of the decoding digital circuits comprises:

a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information;

a digital filter that filters out the adjacent channel information; and

an error correction stage to produce the data packets from the selected channel information.

Claim 17. (Original) The circuit of claim 16 wherein the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel.

Claim 18. (Currently Amended) ~~An integrated~~ The circuit of claim 17 ~~comprising: a single monolithic substrate in which the following circuit components are provided: an input receiving an RF analog signal including a plurality of channels; an analog-to-digital converter to sample and convert the RF analog signal to a digital signal; a first digital tuner that downconverts the digital signal to a first downconverted digital signal, wherein information of a selected first channel in the downconverted digital signal is centered at zero frequency; a first channel decoding digital circuit connected to the first digital tuner that digitally decodes the first downconverted digital signal to output a stream of data packets for the selected first channel; a second digital tuner that downconverts the digital signal to a second downconverted digital signal, wherein information of a selected second channel in the downconverted digital signal is centered at zero frequency; and a second channel decoding digital circuit connected to the second digital tuner that digitally decodes the second downconverted digital signal to output a stream of data packets for the selected second channel; wherein circuitry of the converter, tuners and channel decoding digital circuits are fabricated on that single monolithic substrate;~~ wherein the first and second channel decoding digital circuits each include a digital filter that filters out the adjacent channel information and is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel.

Claim 19. (Canceled).

Claim 20. (Original) The circuit of claim 10 wherein the integrated circuit is a component within a satellite digital television signal receiver.

Claim 21. (Currently Amended) An integrated circuit, comprising:

a single monolithic substrate in which the following circuit components are provided:

an input receiving an RF analog signal including a plurality of channels;

a first analog-to-digital converter to sample and convert the RF analog signal to a first digital signal;

a second analog-to-digital converter to sample and convert the RF analog signal to a second digital signal;

a first digital tuner that downconverts a received digital signal to a first downconverted digital signal, wherein information of a selected first channel in the downconverted digital signal is centered at zero frequency;

a first channel decoding digital circuit connected to the first digital tuner that decodes the first downconverted digital signal to output a stream of data packets for the selected first channel;

a second digital tuner that downconverts a received digital signal to a second downconverted digital signal, wherein information of a selected second channel in the downconverted digital signal is centered at zero frequency;

a second channel decoding digital circuit connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel; and

a switching circuit that selectively couples the first and second digital signals output from the first and second converters to the first and second digital tuners;

each of the first and second channel decoding circuits including a digital filter that filters out the adjacent channel information, that digital filter being a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel;

wherein the converters, tuners, channel decoding digital circuits and switching circuit are fabricated on that single monolithic substrate;

wherein each of the decoding digital circuits comprises:

a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information; and

an error correction stage to produce the data packets from the selected channel information;

wherein the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel.

Claim 22. (Previously Presented) The circuit of claim 21 wherein the first analog-to-digital converter is associated with RF analog signals in a first passband and wherein the second analog-to-digital converter is associated with RF analog signals in a second passband.

Claim 23. (Original) The circuit of claim 22 wherein, if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second digital tuners to the first analog-to-digital converter.

Claim 24. (Original) The circuit of claim 22 wherein, if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second digital tuners to the second analog-to-digital converter.

Claim 25. (Original) The circuit of claim 22 wherein, if the first channel is located in the first passband and the second channel is located in the second passband, the switching circuit selectively couples the first digital tuner to the first analog-to-digital converter and the second digital tuner to the second analog-to-digital converter.

Claim 26. (Original) The circuit of claim 22 wherein, if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit

selectively couples the first digital tuner to the second analog-to-digital converter and the second digital tuner to the first analog-to-digital converter.

Claim 27. (Previously Presented) The circuit of claim 22 further including:

a first filter tuned to the first passband that outputs the RF analog signal to the first analog-to-digital converter; and

a second filter tuned to the second passband that outputs the RF analog signal to the second analog-to-digital converter.

Claim 28. (Previously Presented) The circuit of claim 21 wherein the first and second digital tuners perform frequency transposition and channel selection in a digital domain.

Claim 29. (Previously Presented) The circuit of claim 21 wherein each analog-to-digital converter oversamples the received RF analog signal.

Claim 30. (Previously Presented) The circuit of claim 21 wherein the RF analog signal conveys information for the plurality of channels by digital modulation.

Claim 31. (Previously Presented) The circuit of claim 21 wherein the channels of the RF analog signal applied to each analog-to-digital converter extend over a given frequency span and wherein each analog-to-digital converter oversamples the received RF analog signal at a sampling frequency at least twice the given frequency span.

Claim 32. (Previously Presented) The circuit of claim 31 wherein the RF analog signal comprises a satellite digital television analog signal.

Claims 33-35. (Canceled).

Claim 36. (Currently Amended) An integrated ~~The~~ circuit ~~of claim 21~~ comprising:

a single monolithic substrate in which the following circuit components are provided:

an input receiving an RF analog signal including a plurality of channels;

a first analog-to-digital converter to sample and convert the RF analog signal to a first digital signal;

a second analog-to-digital converter to sample and convert the RF analog signal to a second digital signal;

a first digital tuner that downconverts a received digital signal to a first downconverted digital signal, wherein information of a selected first channel in the downconverted digital signal is centered at zero frequency;

a first channel decoding digital circuit connected to the first digital tuner that decodes the first downconverted digital signal to output a stream of data packets for the selected first channel;

a second digital tuner that downconverts a received digital signal to a second downconverted digital signal, wherein information of a selected second channel in the downconverted digital signal is centered at zero frequency;

a second channel decoding digital circuit connected to the second digital tuner that decodes the second downconverted digital signal to output a stream of data packets for the selected second channel; and

a switching circuit that selectively couples the first and second digital signals output from the first and second converters to the first and second digital tuners;

each of the first and second channel decoding circuits including a digital filter that filters out the adjacent channel information, that digital filter being a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel;

wherein the converters, tuners, channel decoding digital circuits and switching circuit are fabricated on that single monolithic substrate;

further comprising a metal plate attached to a rear surface of the single monolithic substrate to provide a high frequency current spike absorbing capacitor having a first plate formed of the substrate and a second plate formed of the metal plate with an oxide dielectric there between.

Claim 37. (Currently Amended) The circuit of claim 36 ~~21~~ wherein the integrated circuit is a component within a satellite digital television signal receiver.

Claim 38. (Currently Amended) An electronic circuit ~~device~~, comprising:

an integrated circuit embodied on a single monolithic substrate and incorporating:

a multi-channel direct sampling type tuner circuit that receives an RF analog signal composed of several channels and outputs first and second channel digital signals, the tuner circuit including analog filtering circuitry and digital conversion and tuning circuitry;

a first channel decoder circuit that receives the first channel digital signal and outputs a first channel stream of data packets; and

a second channel decoder circuit that receives the second channel digital signal and outputs a second channel stream of data packets;

wherein the analog filtering circuitry of the tuner circuit is fabricated in a first portion of that single monolithic substrate and digital circuitry of the tuner circuit and the first and second channel decoder circuits are fabricated in a second portion of ~~on~~ that single monolithic substrate; and

a semiconducting barrier formed in the single monolithic substrate between the first portion and the second portion to insulate the analog circuitry in the first portion from noise on a supply voltage for the digital circuitry in the second portion;

wherein each of the channel decoder circuits comprises:

a decimator filter that filters the downconverted digital signal to output digital signals relating to the selected channel and adjacent channel information;

a digital filter that filters out the adjacent channel information; and

an error correction stage to produce the data packets from the selected channel information;

wherein the decimator filter is a low pass filter having a cut-off frequency approximately equal to twice a frequency half width of a channel.

Claim 39. (Currently Amended) The circuit ~~device~~ of claim 38 wherein the multi-channel direct sampling type tuner circuit comprises:

at least one analog-to-digital converter to convert the received RF analog signal to a digital signal;

a first digital domain frequency transposition circuit that downconverts the digital signal to the first channel digital signal; and

a second digital domain frequency transposition circuit that downconverts the digital signal to the second channel digital signal.

Claim 40. (Currently Amended) The circuit ~~device~~ of claim 39 wherein the multi-channel direct sampling type tuner circuit comprises a first and second analog-to-digital converter that convert the received RF analog signal to a first and second digital signal, and a switching circuit that selectively couples the first and second digital signals to the first and second digital domain frequency transposition circuits.

Claim 41. (Previously Presented) The circuit of claim 40 wherein the first analog-to-digital converter is associated with RF analog signals in a first passband and wherein the second analog-to-digital converter is associated with RF analog signals in a second passband.

Claim 42. (Previously Presented) The circuit of claim 41 wherein, if the first and second channels are located in the first passband, the switching circuit selectively couples the first and second digital domain frequency transposition circuits to the first analog-to-digital converter.

Claim 43. (Previously Presented) The circuit of claim 41 wherein, if the first and second channels are located in the second passband, the switching circuit selectively couples the first and second digital domain frequency transposition circuits to the second analog-to-digital converter.

Claim 44. (Previously Presented) The circuit of claim 41 wherein, if the first channel is located in the first passband and the second channel is located in the second passband, the switching circuit selectively couples the first digital domain frequency transposition circuit to the first analog-to-digital converter and the second digital domain frequency transposition circuit to the second analog-to-digital converter.

Claim 45. (Previously Presented) The circuit of claim 41 wherein, if the first channel is located in the second passband and the second channel is located in the first passband, the switching circuit selectively couples the first digital domain frequency transposition circuit to the second analog-to-digital converter and the second digital domain frequency transposition circuit to the first analog-to-digital converter.

Claim 46. (Previously Presented) The circuit of claim 41 further including:

a first filter tuned to the first passband that outputs the RF analog signal to the first analog-to-digital converter; and

a second filter tuned to the second passband that outputs the RF analog signal to the second analog-to-digital converter.

Claim 47. (Previously Presented) The circuit of claim 38 wherein the analog-to-digital converter oversamples the received RF analog signal.

Claim 48. (Previously Presented) The circuit of claim 38 wherein the RF analog signal conveys information for the plurality of channels by digital modulation.

Claim 49. (Previously Presented) The circuit of claim 38 wherein the channels of the RF analog signal extend over a frequency span and wherein the analog-to-digital converter oversamples the received RF analog signal at a sampling frequency at least twice the frequency span.

Claim 50. (Previously Presented) The circuit of claim 49 wherein the RF analog signal comprises a satellite digital television analog signal.

Claims 51-52. (Canceled).

Claim 53. (Currently Amended) ~~An electronic~~ The circuit of claim 38 ~~comprising: an integrated circuit embodied on a single monolithic substrate and incorporating: a multi-channel direct sampling type tuner circuit that receives an RF analog signal composed of several channels and outputs first and second channel digital signals; a first channel decoder circuit that receives the first channel digital signal and outputs a first channel stream of data packets; and a second channel decoder circuit that receives the second channel digital signal and outputs a second channel stream of data packets; wherein the tuner circuit and the first and second channel decoder circuits are fabricated on that single monolithic substrate;~~ wherein each of the channel decoder circuits includes a digital filter that filters out the adjacent channel information and is a Nyquist filter having a cut-off frequency approximately equal to the frequency half width of the channel.

Allowance

2. Claims 3, 19, 33-35, 51, & 52 have been cancelled.

3. Claims 1, 2, 4-18, 20-32, 36-50, & 53-55 have been amended with written arguments which overcome the examiner's prior rejections and objections, see paper of 01/22/2009. Examiner withdraws all outstanding rejections and objections to Claims 1, 2, 4-18, 20-32, 36-50, & 53-55.

4. Claims 1, 2, 4-18, 20-32, 36-50, & 53-55 are allowed.

Examiner's Statement of Reasons for Allowance

5. Prior art was found which disclosed direct-conversion tuner integrated circuit for direct broadcast satellite television [e.g. Tomasz et al. (US-6031878-A)] and digital signal processor for multistandard television reception [e.g. Robbins et al. (US-6147713-A)] and pipelined analog-to-digital architecture with parallel-autozero analog signal processing [e.g. Hwang et al. (US-4894657-A)] and filtering arrangement [e.g. Young (EP-0481543-A1)] and transport of payload information and control messages on multiple orthogonal carriers spread throughout substantially all of a frequency bandwith [e.g. Dapper et al. (US-6275990-B1)] and integrated imaging and ranging lidar receiver with ranging information pickoff circuit [e.g. Lieber et al. (US-5220164-A)] and cable receiver IC with integrated decoder [e.g. Tan et al. ("A 70-Mb/s Variable-Rate 1024-QAM Cable Receiver IC with Integrated 10-b ADC and FEC Decoder")] and tuner for digital satellite receiver [e.g. Pugel et al. (US-5654774-A)] and monolithic direct digital receiver; performs coarse tuning; same substrate for analog and digital [e.g. Stehlik (US-5517529-A)] and integrated multi-tuner satellite receiver architecture and associated method [e.g. Khoini-Poorfard et al. (US 7167694 B2)] and isolator and a modem device using the isolator [e.g. Yukutake et al. (US-6603807-B1)] and satellite channel interface in indoor unit used for satellite data communication [e.g. Tonomura (US-5671220)] and cable modem tuner with an upstream and a reception circuit in the same casing [e.g. Matsuura (US-6131023)] and semiconductor device having a plurality of circuits driven by different power sources and formed on the same substrate [e.g. Ono (US-5796147)] and optically patterned RF shield for an integrated circuit chip for analog and/or digital operation at microwave frequencies [e.g. Immorlica et al. (US-5151769)].

6. The following is an examiner's statement of reasons for allowance:

- The prior art of record does not teach or render obvious the limitations as recited in independent Claims 1, 4, 10, 21, 36, 38, & 54 specific to "the tuning circuit comprises: a multibit analog/digital conversion stage having a sampling frequency equal to at least twice the said frequency span of the sampled RF signals" and "the tuning circuit comprises: several digital devices for transposing frequencies that are connected to the output of the analog conversion stage, each digital device configured to separately deliver a sampled digital signal centered around the zero frequency and corresponding to the selected channel" and "each channel decoding circuit comprises: a low pass digital decimator filter followed by an additional digital filter for eliminating information of adjacent channels" and "the additional filter having a cutoff frequency of the order of the frequency half-width of a channel" and "a grounding metal plate glued to a rear face of the single monolithic substrate by a conducting glue to provide a high frequency current spike absorbing capacitor having a first plate formed of the substrate and a second plate formed of the metal plate with an oxide dielectric there between" and "each channel decoding circuit comprises: a digital error correction stage for delivering a stream of data packets corresponding to the information conveyed by the channel associated with the sampled digital signal processed by this channel decoding circuit".
- Dependent claims are allowed as they depend from an allowable independent claim.
- Therefore, the Examiner considers both the combination of the above limitations and the remaining limitations found in each respective independent claim as applied to decoding satellite digital television signals as the non-obvious novelties of the invention.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Oscar Louie whose telephone number is 571-270-1684. The examiner can normally be reached Monday through Thursday from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami, can be reached at 571-272-4195. The fax phone number for Formal or Official faxes to Technology Center 2400 is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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